AMENDMENTS TO THE CLAIMS

1. (Currently amended) A process of forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy, the process comprising:

forming a diffusion barrier layer on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer over the diffusion barrier layer, the diffusion barrier layer located between the first conductive layer and the under bump metallurgy; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the diffusion barrier layer, wherein the second conductive layer has a different composition than the first conductive layer and wherein the first conductive layer does not include material from one of the second conductive layer and the diffusion barrier layer.

2. (Original) The process of Claim 1 wherein the diffusion barrier layer comprises copper or nickel.

3. (Currently amended) The process of Claim 1, wherein the first conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

4. (Original) The process of Claim 3, wherein the first conductive layer comprises tin or silver.

5. (Currently amended) The process of Claim 1, wherein the second conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

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6. (Original) The process of Claim 5, wherein the second conductive layer comprises tin or silver.

7. (Original) The method of Claim 1 further comprising forming at least one additional conductive layer over the diffusion barrier layer.

8. (Currently amended) The method of Claim 7, wherein the at least one additional conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

9. (Original) The method of Claim 1, wherein the diffusion barrier layer is formed by electrolytic deposition.

10. (Original) The method of Claim 1, wherein either the first or the second conductive layer is free of tin and silver.

11. (Currently amended) A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming one of a patterned mask and a diffusion barrier layer over a conductive under bump metallurgy;

forming the other of the patterned mask and the diffusion barrier layer, wherein the pattered mask is formed on the diffusion barrier layer and wherein the diffusion barrier layer is formed on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer on a surface of the ~~microelectronic workpiece~~ diffusion barrier layer; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the

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microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer~~; and~~

~~forming a lead-free third conductive layer over the second conductive layer, the second conductive layer located between the third conductive layer and the first conductive layer, wherein the third conductive layer has a different composition than the second conductive layer~~.

12. (Currently amended) The method of Claim 11, wherein the first[[,]] and second~~, and third~~ conductive layers ~~comprise~~ are selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

13. (Currently amended) The method of Claim 11, wherein the first[[,]] and second~~, and third~~ conductive layers ~~comprise~~ are selected from the group consisting of tin, silver, [[or]] and copper.

14. (Currently amended) The process of Claim 11, further comprising the step of forming at least one additional conductive layer, wherein the at least one additional conductive layer has a different composition than the second conductive layer.

15. (Currently amended) The process of Claim 14, wherein the at least one additional conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

16. (Currently amended) A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming one of a patterned mask and a diffusion barrier layer over a conductive under bump metallurgy;

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forming the other of the patterned mask and the diffusion barrier layer, wherein the pattered mask is formed on the diffusion barrier layer and wherein the diffusion barrier layer is formed on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer on a surface of the ~~microelectronic workpiece~~ diffusion barrier layer; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer, at least one of the first and second conductive layers comprising an alloy of at least two conductive materials.

17. (Currently amended) The process of Claim 16, wherein the first and second conductive layers ~~comprise~~ are selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

18. (Currently amended) The method of Claim 16, wherein the at least two conductive materials are selected from the group consisting of tin, silver, copper, gold, and bismuth.

19. (Original) The method of Claim 16, further comprising forming at least one additional conductive layer over the surface of the microelectronic workpiece.

20. (Currently amended) The method of Claim 19, wherein the additional conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

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21. (Currently amended) A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming one of a patterned mask and a diffusion barrier layer over a conductive under bump metallurgy;

forming the other of the patterned mask and the diffusion barrier layer, wherein the pattered mask is formed on the diffusion barrier layer and wherein the diffusion barrier layer is formed on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer on a surface of the ~~microelectronic workpiece~~ diffusion barrier layer; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer, wherein the second conductive layer is formed by substitutional reduction.

22. (Currently amended) The method of Claim 21, wherein the first and second conductive layers ~~comprise~~ are selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

23. (Original) The method of Claim 21, wherein the first and second conductive layers comprise tin or silver.

24. (Original) The method of Claim 21 further comprising the step of forming at least one additional conductive layer over the microelectronic workpiece.

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25. (Currently amended) The process of Claim 24, wherein the at least one additional conductive layer ~~comprises~~ is selected from the group consisting of tin, silver, copper, gold, [[or]] and bismuth.

26. (Currently amended) The method of Claim 21, wherein the second layer ~~comprises~~ is selected from the group consisting of silver, copper, gold, [[or]] and bismuth.

27-41. (Canceled)

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